IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Masumitsu Ino et al.

Application No.: 09/424,544 Confirmation No.: 8128

Filed: November 24, 1999 Art Unit: 2673

For: LIQUID CRYSTAL DISPLAY Examiner: J. J. Piziali

RESPONSE TO NOTICE OF NON-COMPLIANT APPEAL BRIEF (37 C.F.R. 41.37)

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This is in response to the Notice of Non-Compliant Appeal Brief (37 C.F.R. 41.37) mailed on July 21, 2006. A Supplemental Appellant's Brief is provided in response to the Notice.

Appreciation is expressed to the Examiner for extending the courtesy of an interview on August 16, 2006 to discuss the Notice of Non-Compliant Appeal Brief (37 C.F.R. 41.37) mailed on July 21, 2006. The Examiner discussed his reasoning for the objections raised within the Notice. However, *no agreement* was reached during the interview regarding the propriety of the objections raised within the Notice.

Nevertheless, while not conceding the propriety of the objections raised within the Notice and in order to advance the prosecution of the above-identified application, the previous Appeal Brief of December 13, 2005 has been modified in accordance with the suggestions provided by the Examiner during the interview of August 16, 2006.

Specifically, Section III of the instant Supplemental Appellant's Brief has been modified with the Examiner's assistance in a manner that would include incorporating a status identifier of "objected to" for claims 13 and 14 along with the other status identifiers previously attributed to those claims within the Appeal Brief of December 13, 2005.

Section III of the instant Supplemental Appellant's Brief has been further modified as suggested by the Examiner to include the statement "Accordingly, Appellant hereby appeals the final rejection of claims 3, 5-7, 11, 13-20, 23-29, 31, 37, and 43-48 which are presented in the Claims Appendix."

Within the Notice of Non-Compliant Appeal Brief (37 C.F.R. 41.37) of July 21, 2006 and during the Interview of August 16, 2006, the Examiner now indicates that no entry of U.S. Patent No. 6,788,380 to Melnik et al. has been found within the record and requests the removal from the Appeal Brief of the citation to this document. This removal has been requested by the Examiner notwithstanding the presence of a citation to this document within the previous Appeal Brief of October 29, 2004 and notwithstanding the absence of any objection to a citation of this document within the previous Notice of Non-Compliant Appeal Brief (37 C.F.R. 41.37) dated November 21, 2005.

The Notice of Non-Compliant Appeal Brief (37 C.F.R. 41.37) of July 21, 2006 further contends that no copy of Melnik et al. has been filed along with the Appeal Brief of December 13, 2005.

However, a postcard receipt was presented on December 13, 2005 along with the Appeal Brief and stamped with the Office Date stamp of December 13, 2005. A copy of the postcard receipt bearing the Office Date stamp of December 13, 2005 is provided along with this Response as ATTACHMENT A.

The USPTO has a well-established and well-published practice of providing a receipt for papers filed in the USPTO to any applicant desiring a receipt. This practice requires that any paper for which a receipt is desired be filed in the USPTO with a postcard identifying the paper. A

postcard receipt that itemizes and properly identifies the papers that are being filed serves as *prima facie* evidence of receipt in the USPTO. See M.P.E.P. §505.

In this regard, the postcard receipt bearing the Office Date stamp of December 13, 2005 itemizes and properly identifies U.S. Patent No. 6,788,380 to Melnik et al. that has been alleged by the Notice of July 21, 2006 to be missing. Nevertheless, the citation of U.S. Patent No. 6,788,380 to Melnik et al. has been removed from the instant Supplemental Appellant's Brief, as requested.

Within the Notice of Non-Compliant Appeal Brief (37 C.F.R. 41.37) of July 21, 2006 and during the Interview of August 16, 2006, the Examiner has indicated that entry of neither *Verdegaal Bros., Inc. v. Union Oil Co.,* 814 F.2d 628, 2 USPQ2d 1051 (Fed. Cir. 1987) nor *Trintec Indus., Inc. v. Top-U.S.A. Corp.*, 295 F.3d 1292, 63 USPQ2d 1597 (Fed. Cir. 2002) has been found within the record and has requested the removal from the Appeal Brief of the citation to these Federal Circuit authorities from the Evidence Appendix. In response, the citations to these Federal Circuit authorities have been removed from the instant Supplemental Appellant's Brief, as requested.

If any fee is required or any overpayment made, the Commissioner is hereby authorized to charge the fee or credit the overpayment to Deposit Account # 18-0013.

Dated: August 17, 2006

Respectfully submitted,

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ATTACHMENT A

Inventor: Masumitsu Ino et al.

Atty Docket No.: SON-1582/SUG
(80001-1582)

Application No.: 09/424,544-Cont-[illegible]128

Filing Date: November 24, 1999

Title: LIQUID CRYSTAL DISPLAY

Documents Filed:

Response to Notice of Non-Compliant Appeal Brief (1 page)

Supplemental Appealant's Brief (27 pages)

Reference(s): US 6,788,380

Verdegaal Brothers Inc. v. Union Oil Co. of California

Trintec Industries Inc. v. Top-U.S.A. Corp.

Via: Courier

Sender's Initials: RPK/BKD/kas

Date: December 13, 2005

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Masumitsu Ino et al.

Application No.: 09/424,544 Confirmation No.: 8128

Filed: November 24, 1999 Art Unit: 2673

For: LIQUID CRYSTAL DISPLAY Examiner: J. J. Piziali

SUPPLEMENTAL APPELLANT'S BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This is an Appeal Brief under 37 C.F.R. §41.37 appealing the final decision of the Examiner dated November 4, 2003. Each of the topics required by 37 C.F.R. §41.37 is presented herewith and is labeled appropriately.

This brief is in furtherance of the Final Office Action on November 4, 2003.

A Notice of Appeal was filed in this case on February 4, 2004.

I. REAL PARTY IN INTEREST

Sony Corporation of Tokyo, Japan ("Sony") is the real party in interest of the present application. An assignment of all rights in the present application to Sony was executed by the inventor and recorded by the U.S. Patent and Trademark Office at **reel 010555, frame 0866.**

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

Claims 1-20 were originally filed in this application.

By the amendment filed on February 27, 2002, claims 9 and 16 have been amended, and claims 21-39 added.

By the amendment filed on September 16, 2002, claims 3 and 38 have been amended, and claims 40-42 added.

By the amendment filed on February 26, 2003, claims 1-2, 10, 12-13, 21-22, 30, 32-36, and 38-42 have been canceled, claims 3, 11, 13, 15, 17-20, 25-27 and 37 have been amended, and claims 43-48 added.

By the amendment filed on August 20, 2003, claim 3 has been amended.

Within the Final Office Action of November 4, 2003:

- Paragraph 4 indicates that claim 13 has been objected to.
- Paragraph 5 indicates that claim 14 has been objected to.
- Paragraph 7 indicates that claims 3, 5-7, 11, 13-20, 23-29, 31, 37, and 43-48 are rejected under 35 U.S.C. §102 as allegedly being anticipated by U.S. Patent 4,825,203 issued to Takeda et al. (Takeda).

Thus, the status of the claims is as follows:

Claims 1-2 (canceled)

Claim 3 (rejected)

Claim 4 (canceled)

Claims 5-7 (rejected)

Claims 8-10 (canceled)

Claim 11 (rejected)

Claim 12 (canceled)

Claim 13 (rejected and objected to)

Claim 14 (rejected and objected to)

Claims 15-20 (rejected)

Claims 21-22 (canceled)

Claims 23-29 (rejected)

Claim 30 (canceled)

Claim 31 (rejected)

Claims 32-36 (canceled)

Claim 37 (rejected)

Claims 38-42 (canceled)

Claims 43-48 (rejected)

Pursuant to M.P.E.P. §706.01, the objection to claims 13 and 14 found within paragraphs 4 and 5 of the Final Office Action may be reviewed only by way of petition. Accordingly, the objection to claims 13 and 14 is not the subject of this appeal.

No claims are indicated within the Final Office Action to contain allowable subject matter.

Accordingly, Appellant hereby appeals the final rejection of claims 3, 5-7, 11, 13-20, 23-29, 31, 37, and 43-48 which are presented in the Claims Appendix.

IV. STATUS OF AMENDMENTS

Subsequent to the final rejection of November 4, 2003, an Amendment After Final Action (37 CFR Section 1.116) has been filed on February 4, 2004.

The Advisory Action of February 25, 2004 indicated that the Amendment After Final Rejection Under 37 C.F.R. § 1.116 of February 4, 2004 had not been entered.

A Second Amendment After Final Rejection Under 37 C.F.R. § 1.116 and a Third Amendment After Final Rejection Under 37 C.F.R. § 1.116 have been filed on March 8, 2004.

The Advisory Action of July 21, 2004 indicated that the Second and Third Amendments After Final Rejection Under 37 C.F.R. § 1.116 had not been entered.

The Fourth and Fifth Amendments After Final Rejection Under 37 C.F.R. § 1.116 have been filed have been filed on July 22, 2004

The Advisory Action of October 21, 2004 indicated that the Fourth and Fifth Amendments After Final Rejection Under 37 C.F.R. § 1.116 had not been entered.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The present invention relates to a liquid crystal display (LCD) and, more particularly, to a matrix type liquid crystal display in which a driver circuit to apply a signal potential to each pixel is provided as an external circuit of a liquid crystal display panel.

Claims 3, 5, 7, 11, 13-20 and 23-24 - Claims 5, 7, 11, 13-20 and 23-24 are dependent upon claim 3. Claim 3 is drawn to a liquid crystal display comprising:

> a display portion 10 (specification at figure 6) in which a plurality of pixels are two-dimensionally arranged at intersecting points of gate lines 41 as many as a plurality of rows and signal lines 42 as many as a plurality of columns which are wired in a matrix shape (specification at figure 7, page 18, lines 20-27);
>
> a plurality of driver circuits 44 for applying a signal potential to each pixel in said display portion through the signal lines 42 of said plurality of columns (specification at figure 7, page 19, lines 16-21); and
>
> time-divisional switches 46 for time-divisionally sending a signal potential that is outputted from each of said plurality of driver circuits 44 to the signal lines 42 of said plurality of columns (specification at figures 7-9, page 20, line 25 to page 23, line 21),
>
> characterized in that a time-dividing number of said time-divisional switches 46 is equal to 3 (specification at page 36, line 27),
>
> the number of output terminals 45 of each of said plurality of driver circuits 44 is set to a measure of the total number of signal lines 42 of said plurality of columns,

the number of output terminals of each of said plurality of driver circuits is set to a same number (specification at figure 8, page 21, lines 14-24),

when a size of a frame portion adjacent to said display portion is specified, the number (n) of output terminals of each of said plurality of driver circuits is determined on the basis of said specified frame size by the number of lines which can be wired into a wiring region of said frame portion (specification at page 44, line 17 to page 45, line 4),

when the total number of signal lines of said plurality of columns that is decided by a display system is set to N, the number of said driver circuits is set to N/n, said total number of signal lines being different than said number (n) of output terminals (specification at page 44, lines 23-26).

Claim 6 - Claim 6 is dependent upon claim 3. Within claim 6, said plurality of driver circuits 44 are driver ICs arranged in an outside of a transparent insulating substrate on which said display portion 10 is formed (specification at figure 6).

Claims 25-29, 37, 43-47 - Claims 29, 37, 43-47 are dependent upon claim 25. Claim 25 includes the features of:

a display portion 10 (specification at figure 5), said display portion 10 having a plurality of gate lines 11, a plurality of signal lines 12 and a plurality of pixels 20 (specification at figure 3, page 9, lines 5-17),

a pixel 20 of said plurality of pixels 20 being located at an intersection of a gate line 11 of said plurality of gate lines 11 and a signal line 12 of said plurality of signal lines 12 (specification at figure 3); and

a plurality of driver circuits 14, 44 (specification at page 19, lines 5-6), said plurality of driver circuits 14, 44 including at least one general driver circuit and one remainder driver circuit (specification at figure 5),

each said at least one general driver circuit 14, 44 having a plurality of general driver circuit output terminals, a general driver circuit output terminal of said plurality of general driver circuit output terminals 14, 44 providing a signal potential to one of said plurality of signal lines (specification at page 19, lines 5-6),

said remainder driver circuit having a plurality of remainder driver circuit output terminals, a remainder driver circuit output terminal of said plurality of remainder driver circuit output terminals providing another signal potential to another of said plurality of signal lines (specification at figure 5),

the quantity of remainder driver circuit output terminals being defined as (S – (OP * (DC-1))) (specification at figure 5, page 13, lines 18-21), "S" being the quantity of said plurality of signal lines 12 (specification at page 13, lines 10-13), "OP" being the quantity of general driver circuit output terminals, and "DC" being the quantity of said plurality of driver circuits 14 (specification at figure 5, page 13, lines 21-26),

said quantity of general driver circuit output terminals being different than said quantity of remainder driver circuit output terminals (specification at figure 5).

Claim 31 - Claim 31 is dependent on claim 25. Claim 31 includes a surplus connecting region that does not contribute to said display portion does not occur on the said display (specification page 16, lines 22-24).

Claim 48 - Claim 48 is dependent upon claim 25. Within claim 48, the plurality of driver circuits are driver integrated circuits arranged in an outside of a transparent insulating substrate on which said display portion is formed (specification at figure 5).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The issues presented for consideration in this appeal are as follows:

Whether the Examiner erred in rejecting claims 3, 5-7, 11, 13-20, 23-29, 31, 37, 43-48 were rejected under 35 U.S.C. 102 as allegedly being anticipated by U.S. Patent 4,825,203 issued to Takeda et al. (Takeda).

This issue will be discussed hereinbelow.

VII. ARGUMENT

In the Office Action of November 4, 2003:

The Examiner rejected claims 3, 5-7, 11, 13-20, 23-29, 31, 37, 43-48 under 35 U.S.C. 102 as allegedly being anticipated by Takeda.

For at least the following reasons, Appellant submits that this rejection is both technically and legally unsound and should therefore be reversed.

For purposes of this appeal brief only, and without conceding the teachings of any prior art reference, the claims have been grouped as indicated below.

Claim Groups:

Claims 3, 5, 7, 11, 13-20 and 23-24 stand or fall together.

Claim 6 stands or falls separately.

Claim 25-29, 37, 43-47 stand or fall together.

Claim 31 stands or falls separately.

Claim 48 stands or falls separately.

The Examiner erred in rejecting claims 3, 5-7, 11, 13-20, 23-29, 31, 37, 43-48 under 35 U.S.C. 102 as allegedly being anticipated by Takeda.

Claims 3, 5, 7, 11, 13-20 and 23-24

This rejection of these claims is respectfully traversed for at least the following reasons.

A claim is anticipated only if *each and every element* as set forth in the claim is found, *either expressly or inherently* described, in a single prior art reference.

Claims 5, 7, 11, 13-20 and 23-24 are dependent upon claim 3. Claim 3 is drawn to a liquid crystal display comprising:

> a display portion 10 (specification at figure 6) in which a plurality of pixels are two-dimensionally arranged at intersecting points of gate lines 41 as many as a plurality of rows and signal lines 42 as many as a plurality of columns which are wired in a matrix shape (specification at figure 7, page 18, lines 20-27);
>
> a plurality of driver circuits 44 for applying a signal potential to each pixel in said display portion through the signal lines 42 of said plurality of columns (specification at figure 7, page 19, lines 16-21); and
>
> time-divisional switches 46 for time-divisionally sending a signal potential that is outputted from each of said plurality of driver circuits 44 to the signal lines 42 of said plurality of columns (specification at figures 7-9, page 20, line 25 to page 23, line 21),
>
> characterized in that a time-dividing number of said time-divisional switches 46 is equal to 3 (specification at page 36, line 27),

the number of output terminals 45 of each of said plurality of driver circuits 44 is set to a measure of the total number of signal lines 42 of said plurality of columns,

the number of output terminals of each of said plurality of driver circuits is set to a same number (specification at figure 8, page 21, lines 14-24),

when a size of a frame portion adjacent to said display portion is specified, the number (n) of output terminals of each of said plurality of driver circuits is determined on the basis of said specified frame size by the number of lines which can be wired into a wiring region of said frame portion (specification at page 44, line 17 to page 45, line 4),

when the total number of signal lines of said plurality of columns that is decided by a display system is set to N, the number of said driver circuits is set to N/n, said total number of signal lines being different than said number (n) of output terminals (specification at page 44, lines 23-26).

Within the claims, the total number of signal lines is different than the number (n) of output terminals of each of the plurality of driver circuits.

Regarding the use of Takeda, calculations provided within the Office Action arguably teach the total number of signal lines in Takeda being ***the same as*** the number (n) of output terminals of each of the plurality of driver circuits.

However, the claimed invention provides that the total number of signal lines ***is different than*** the number (n) of output terminals of each of the plurality of driver circuits.

Thus, all claimed features are not found within Takeda.

Claim 6

In addition to the reasons provided hereinabove with respect to the rejection of claim 3, the rejection of claim 6 is respectfully traversed for at least the following reasons.

Within claim 6, said plurality of driver circuits 44 are driver ICs arranged in an outside of a transparent insulating substrate on which said display portion 10 is formed (specification at figure 6).

As a rule, a claim is anticipated only if *each and every element* as set forth in the claim is found, *either expressly or inherently* described, in a single prior art reference.

However, a review of Takeda reveals that a "substrate" is not found therein. In addition, Takeda is silent as to the substrate being a "transparent insulating substrate".

Thus, Takeda *fails to expressly* teach that a plurality of driver circuits are driver ICs arranged in an outside of a *transparent insulating substrate* on which the display portion is formed.

Also as a rule, *inherent* anticipation requires that the missing descriptive material is "*necessarily present*," not merely probably or possibly present, in the prior art.

Here, the Final Office Action *fails* to show that **a transparent insulating substrate is *"necessarily present"*** within Takeda.

Because a "substrate" or a "transparent insulating substrate" is not found within Takeda, all features within claim 6 are not found within Takeda, and because a transparent insulating substrate is not inherent, the final rejection of at least claim 6 is improper and premature as a result.

In addition, rejected claim 6 provide that when a size of a frame portion adjacent to the display portion is specified, the number (n) of output terminals of each of the plurality of driver circuits is determined on the basis of the specified frame size by the number of lines which can be wired into a wiring region of the frame portion, and when the total number of signal lines of the plurality of columns that is decided by a display system is set to N, the number of the driver circuits is set to N/n, the total number of signal lines being different than the number (n) of output terminals.

The Final Office Action cites elements q_1-q_N of Takeda as the plurality of driver circuits. While figure 1(A) of Takeda arguably depicts elements q_1-q_N at the output of shift register 31, the description found within Takeda fails to provide, with particularity, a written definition for elements q_1-q_N.

Instead, Takeda arguably teaches that "the column electrode drive circuit mainly comprises a shift register (31) which outputs a signal corresponding to the display pattern to each column electrode line" (figures 1(A),(B), column 4, lines 29-31), that "the signals required for sequential display are input to the gate circuit (37) from the shift register" (column 4, lines 59-61), and that "a shift register (31) that outputs signals to each column electrode line corresponding to the display pattern" (figure 5(A), column 6, lines 12-14). As shown above, Takeda arguably teaches elements q_1-q_N as "signals" while failing to disclose, teach or suggest elements q_1-q_N as "a plurality of driver circuits".

Moreover, calculations provided within the Final Office Action arguably teach the total number of signal lines in Takeda as being ***the same as*** the number (n) of output terminals of each of the plurality of driver circuits. However, the claimed invention provides that the total number of signal lines ***is different*** than the number (n) of output terminals of each of the plurality of driver circuits.

Claims 25-29, 37, 43-47

A claim is anticipated only if *each and every element* as set forth in the claim is found, *either expressly or inherently* described, in a single prior art reference.

Claim 25 includes the features of:

a display portion 10 (specification at figure 5), said display portion 10 having a plurality of gate lines 11, a plurality of signal lines 12 and a plurality of pixels 20 (specification at figure 3, page 9, lines 5-17),

a pixel 20 of said plurality of pixels 20 being located at an intersection of a gate line 11 of said plurality of gate lines 11 and a signal line 12 of said plurality of signal lines 12 (specification at figure 3); and

a plurality of driver circuits 14, 44 (specification at page 19, lines 5-6), said plurality of driver circuits 14, 44 including at least one general driver circuit and one remainder driver circuit (specification at figure 5),

each said at least one general driver circuit 14, 44 having a plurality of general driver circuit output terminals, a general driver circuit output terminal of said plurality of general driver circuit output terminals 14, 44 providing a signal potential to one of said plurality of signal lines (specification at page 19, lines 5-6),

said remainder driver circuit having a plurality of remainder driver circuit output terminals, a remainder driver circuit output terminal of said plurality of remainder driver circuit output terminals providing another signal potential to another of said plurality of signal lines (specification at figure 5),

the quantity of remainder driver circuit output terminals being defined as (S – (OP * (DC-1))) (specification at figure 5, page 13, lines 18-21), "S" being the quantity of said plurality of signal lines 12 (specification at page 13, lines 10-13), "OP" being the quantity of general driver circuit output terminals, and "DC" being the quantity of said plurality of driver circuits 14 (specification at figure 5, page 13, lines 21-26),

said quantity of general driver circuit output terminals being different than said quantity of remainder driver circuit output terminals (specification at figure 5).

Claim 25 and the claims dependent thereon comprise a plurality of driver circuits including at least one general driver circuit wherein a general driver circuit output terminal provides a signal potential to one of the plurality of signal lines. The plurality of driver circuits further

includes one remainder driver circuit wherein a remainder driver circuit output terminal provides another signal potential to another of the plurality of signal lines.

The Final Office Action contends that Takeda depicts row electrodes 11-a as a plurality of gate lines 11-a and column electrodes 11-b as a plurality of signal lines 11-b. Thus, the Final Office Action identifies the row electrodes 11-a as the plurality of gate lines 11-a, and not as the plurality of signal lines.

But while figure 1(A) of Takeda arguably depicts plurality of driver circuits having a column electrode drive circuit 13 (column 4, line 23) providing signals to column electrodes 11-b (column 3, lines 4-6), and figure 3(A) of Takeda arguably depicts a row electrode drive circuit 121,122 (column 4, lines 11-12) providing signals to row electrodes 11-a (column 3, lines 1-2), Takeda fails to disclose, teach or suggest both the column electrode drive circuit 13 and the row electrode drive circuit 121,122 providing signal potentials to column electrodes 11-b.

Thus, Takeda fails to disclose, teach or suggest column electrode drive circuit 13 and the row electrode drive circuit 121,122 as the plurality of driver circuits found within claim 25 and the claims dependent thereon since the claimed plurality of driver circuits provide a signal potential to the plurality of signal lines whereas the row electrode drive circuit 121,122 of Takeda provides signal potentials to the row electrodes 11-a and not to the column electrodes 11-b.

The Final Office Action cites elements q_1-q_N of Takeda as the plurality of driver circuits. While figure 1(A) of Takeda arguably depicts elements q_1-q_N at the output of shift register 31, the description found within Takeda fails to provide, with particularity, a written definition for elements q_1-q_N. Instead, Takeda arguably teaches that "the column electrode drive circuit mainly comprises a shift register (31) which outputs a signal corresponding to the display pattern to each column electrode line" (figures 1(A),(B), column 4, lines 29-31), that "the signals required for sequential display are input to the gate circuit (37) from the shift register" (column 4, lines 59-61), and that "a shift register (31) that outputs signals to each column electrode line corresponding to the display pattern" (figure 5(A), column 6, lines 12-14). As shown above, Takeda arguably teaches elements

q_1-q_N as "signals" while failing to disclose, teach or suggest elements q_1-q_N as "a plurality of driver circuits".

Also note that figure 1(A) of Takeda depicts buffer 36 as having only a single output Q_N, and not two (2) outputs as contended within the Office Action, and that a single signal q_N shown within figure 1(A) of Takeda corresponds only to a single output Q_N.

Moreover, claim 25 and the claims dependent thereon provide that the quantity of general driver circuit output terminals are different than the quantity of remainder driver circuit output terminals. But as shown within figure 1(A) there is the same quantity of outputs from each of the buffers 36, there is the same quantity of outputs from each of the analog switches 32, 34, and there is the same quantity of outputs from each of the gate circuits 37.

The Final Office Action further contends that each general driver circuit has a plurality of general driver circuit output terminals 36. But since each of the signals q_1-q_N of Takeda are uniquely associated with a buffer 36, this contention is inconsistent at least with the other contention regarding claim 25 made within the Final Office Action that elements q_1-q_N of Takeda are the plurality of driver circuits.

The Final Office Action asserts without provided any evidentiary support that there are two (2) remainder driver circuit output terminals, five (5) plurality of signal lines, three (3) general driver circuit output terminals, and two (2) plurality of driver circuits.

In response, this unsupported assertion amounts to nothing more than conclusions that are personal in nature because the cited prior art does not contain a sufficient teaching of how to obtain the desired result, or that the claimed result would be obtained if certain directions were pursued. In this regard, the teachings, suggestions or incentives supporting the rejection must be clear and particular.

Claim 31

The rejection of this claim is traverse at least for the reasons provided hereinabove with respect to claim 25 and for the following reasons.

A claim is anticipated only if *each and every element* as set forth in the claim is found, *either expressly or inherently* described, in a single prior art reference.

Claim 31 includes a surplus connecting region that does not contribute to said display portion does not occur on the said display (specification page 16, lines 22-24).

However, Takeda fails to disclose, teach or suggest a surplus connecting region that does not contribute to the display portion which does not occur on the display. The Final Office Action cites elements 12, 13 and 15 of Takeda for this teaching. But in this regard, element 12 of Takeda contributes to the display portion as the row electrode drive circuit (Takeda at column 3, line 1), element 13 of Takeda contributes to the display portion as the column electrode drive circuit (Takeda at column 3, line 4), and element 15 of Takeda contributes to the display portion as the control circuit (Takeda at column 3, line 8).

Claim 48

The rejection of this claim is traverse at least for the reasons provided hereinabove with respect to claim 25 and for the following reasons.

Within claim 48, the plurality of driver circuits are driver integrated circuits arranged in an outside of a transparent insulating substrate on which said display portion is formed (specification at figure 5).

As a rule, a claim is anticipated only if *each and every element* as set forth in the claim is found, *either expressly or inherently* described, in a single prior art reference.

However, a review of Takeda reveals that a "substrate" is not found therein. In addition, Takeda is silent as to the substrate being a "transparent insulating substrate".

Thus, Takeda *fails to expressly* teach that a plurality of driver circuits are driver ICs arranged in an outside of a *transparent insulating substrate* on which the display portion is formed.

Also as a rule, *inherent* anticipation requires that the missing descriptive material is "*necessarily present*," not merely probably or possibly present, in the prior art.

Here, the Final Office Action *fails* to show that **a transparent insulating substrate is "*necessarily present*"** within Takeda.

Because a "substrate" or a "transparent insulating substrate" is not found within Takeda, all features within claim 48 are not found within Takeda, and because a transparent insulating substrate is not inherent, the final rejection of at least claim 48 is improper and premature as a result.

Conclusion

The Office Action fails to show that **each and every element** as set forth in the claim is found, either expressly or inherently described, solely within Takeda, **which is a specific requirement of an anticipation rejection made pursuant to 35 U.S.C. §102.**

Accordingly, Takeda does not anticipate Applicant's invention. The claims are considered allowable for the same reasons discussed above, as well as for the additional features they recite.

Reversal of the Examiner's decision is respectfully requested.

A copy of the claims involved in the present appeal is attached hereto as the Claims Appendix.

If any fee is required or any overpayment made, the Commissioner is hereby authorized to charge the fee or credit the overpayment to Deposit Account # 18-0013.

Dated: August 17, 2006

Respectfully submitted,

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CLAIMS APPENDIX

1-2 (canceled).

3. (previously presented) A liquid crystal display comprising:

a display portion in which a plurality of pixels are two-dimensionally arranged at intersecting points of gate lines as many as a plurality of rows and signal lines as many as a plurality of columns which are wired in a matrix shape;

a plurality of driver circuits for applying a signal potential to each pixel in said display portion through the signal lines of said plurality of columns; and

time-divisional switches for time-divisionally sending a signal potential that is outputted from each of said plurality of driver circuits to the signal lines of said plurality of columns,

characterized in that a time-dividing number of said time-divisional switches is equal to 3,

the number of output terminals of each of said plurality of driver circuits is set to a measure of the total number of signal lines of said plurality of columns,

the number of output terminals of each of said plurality of driver circuits is set to a same number,

when a size of a frame portion adjacent to said display portion is specified, the number (n) of output terminals of each of said plurality of driver circuits is determined on the basis of said specified frame size by the number of lines which can be wired into a wiring region of said frame portion,

when the total number of signal lines of said plurality of columns that is decided by a display system is set to N, the number of said driver circuits is set to N/n, said total number of signal lines being different than said number (n) of output terminals.

4. (canceled).

5. (original) A display according to claim 3, characterized in that the number of output terminals of each of said plurality of driver circuits is set to a power of 2.

6. (original) A display according to claim 3, characterized in that said plurality of driver circuits are driver ICs arranged in an outside of a transparent insulating substrate on which said display portion is formed.

7. (original) A display according to claim 3, characterized by comprising:

a memory circuit for temporarily storing data to be written into said plurality of driver circuits; and

a control circuit for controlling said plurality of driver circuits so as to simultaneously write different data from said memory circuit.

8-10. (canceled).

11. (previously presented) A display according to claim 3, characterized in that a leading waveform and a trailing waveform of a signal output waveform of each of said plurality of driver circuits are symmetrical with respect to a time base.

12. (canceled).

13. (previously presented) A display according to claim 3, characterized in that a period of time which is selected by said time-divisional switches is equal to or shorter than 1/3 of a horizontal scanning period.

14. (original) A display according to claim 13, characterized in that a leading time and a trailing time of each of said plurality of driver circuits are equal to or shorter than the period of time which is selected by said time-divisional switches.

15. (previously presented) A display according to claim 3, characterized in that a blanking period which is caused for the period of time, selected by said time-divisional switches is equal to or shorter than (a horizontal scanning period – the period of time selected by the time-divisional switches x 3) / 3.

16. (previously presented) A display according to claim 15, characterized in that said plurality of driver circuits have a function to stop the operation of an output circuit of said plurality of driver circuits for said blanking period.

17. (previously presented) A display according to claim 3, characterized in that said plurality of driver circuits generate a signal potential so as to correct curves of voltage-transmittance characteristics of R (red), G (green), and G (blue) by diving to said time-divisional switches.

18. (previously presented) A display according to claim 3, characterized in that in a 1H (H denotes a horizontal scanning period) inversion driving or a 1H common inversion driving, the signal line which is selected first by said time-divisional switches is a line of blue, the signal line which is selected at the second time is a line of green, and the signal line which is selected at the third time is a line of red.

19. (previously presented) A display according to claim 3, characterized in that in a dot inversion driving, the signal line which is selected first by said time-divisional switches is a line of red, the signal line which is selected at the second time is a line of green, and the signal line which is selected at the third time is a line of blue.

20. (previously presented) A display according to claim 3, characterized in that time-division of said time-division switches distribute signals to R (red), G (green), and G (blue) constituting one pixel.

21-22. (canceled).

23. (previously presented) A display according to claim 3, characterized in that a surplus connecting region that does not contribute to said display portion does not occur on the said display.

24. (previously presented) A display according to claim 3, characterized in that a driver circuit of said plurality of driver circuits is separate and distinct from another driver circuit of said plurality of driver circuits.

25. (previously presented) A liquid crystal display comprising:

a display portion, said display portion having a plurality of gate lines, a plurality of signal lines and a plurality of pixels,

a pixel of said plurality of pixels being located at an intersection of a gate line of said plurality of gate lines and a signal line of said plurality of signal lines; and

a plurality of driver circuits, said plurality of driver circuits including at least one general driver circuit and one remainder driver circuit,

each said at least one general driver circuit having a plurality of general driver circuit output terminals, a general driver circuit output terminal of said plurality of general driver circuit output terminals providing a signal potential to one of said plurality of signal lines,

said remainder driver circuit having a plurality of remainder driver circuit output terminals, a remainder driver circuit output terminal of said plurality of remainder driver circuit output terminals providing another signal potential to another of said plurality of signal lines,

the quantity of remainder driver circuit output terminals being defined as (S – (OP * (DC-1))), "S" being the quantity of said plurality of signal lines, "OP" being the quantity of general driver circuit output terminals, and "DC" being the quantity of said plurality of driver circuits,

said quantity of general driver circuit output terminals being different than said quantity of remainder driver circuit output terminals.

26. (previously presented) A display according to claim 25, wherein each driver circuit of said plurality of driver circuits is separate and distinct from another driver circuit of said plurality of driver circuits.

27. (previously presented) A display according to claim 25, wherein said plurality of pixels is arranged in a two-dimensional matrix shape.

28. (previously presented) A display according to claim 25, wherein said pixel of said plurality of pixels includes a transistor, a gate electrode of said transistor being electrically connected to said gate line, a source/drain of said transistor being electrically connected to said signal line.

29. (previously presented) A display according to claim 25, wherein said plurality of gate lines is a plurality of rows and said plurality of signal lines is a plurality of columns.

30. (canceled).

31. (previously presented) A display according to claim 25, wherein a surplus connecting region that does not contribute to said display portion does not occur on the said display.

32-36. (canceled).

37. (previously presented) A display according to claim 25, wherein an output terminal of said plurality of driver circuits is electrically connected to an input terminal of a time-divisional switch, said time-divisional switch providing a de-multiplexed signal potential to said signal line, said de-multiplexed signal potential being a signal potential for one of a plurality of primary colors that is time-divided from another signal potential for another of said plurality of primary colors and supplied to said signal line.

38-42. (canceled).

43. (previously presented) A display according to claim 37, wherein said plurality of primary colors is a first primary color, a second primary color and a third primary color.

44. (previously presented) A display according to claim 25, wherein said quantity of general driver circuit output terminals is greater than said quantity of remainder driver circuit output terminals.

45. (previously presented) A display according to claim 25, wherein the sum total of general driver circuit output terminals and said remainder driver circuit output terminals is equal to said plurality of signal lines.

46. (previously presented) A display according to claim 25, wherein said plurality of driver circuits include more than one said general driver circuit.

47. (previously presented) A display according to claim 46, wherein each said general driver circuit has an equal number of general driver circuit output terminals.

48. (previously presented) A display according to claim 25, wherein said plurality of driver circuits are driver integrated circuits arranged in an outside of a transparent insulating substrate on which said display portion is formed.

EVIDENCE APPENDIX

There is no other evidence which will directly affect or have a bearing on the Board's decision in this appeal.

RELATED PROCEEDINGS APPENDIX

There are no other appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.